A 1-5GHz Low-Power Single-Chip Receiver IC for Optical Video Distribution System

Tatsuto Oka, Taichi Ikedo, Kazuhiro Nojima, and Kazuhisa Fujimoto

Corporate Engineering Division, Matsushita Communication Industrial Co., Ltd.
600, Saedo-cho, Tsuzuki-ku, Yokohama, 224-8539, Japan

***Abstract*—A 1-5GHz low-power single-chip receiver IC has been developed for an optical video signal distribution system. A preamplifier and delay-line type FM demodulator are integrated on to a single-chip using 0.5μm Si-bipolar technology. Using this IC, 80 carriers of 64-QAM digital video signals can be successfully transmitted with bit error rates less than $1x10^{-10}$. This IC operates with low power consumption of 0.7W, which is one of the lowest power consumption figures ever reported for such a device.**

I. INTRODUCTION

Due to the ever-increasing usage of the Internet, the demand for high speed and large capacity communication networks has been continually increasing. The fiber to the home (FTTH) system is one of the most attractive approaches to help realize multimedia networks.

Fig.1 shows the block diagram of an optical video signal distribution system using a super wideband frequency modulation scheme [1]. In this system, FDM video signals are converted to a wideband FM. Next, through the use of passive double star (PDS) networks, an optical signal is distributed to every home. Finally, a FM signal is demodulated back to the original FDM video signals by the optical network unit (ONU) in the home. This system has the advantage of robustness against noise. For the ONU, broadband operation is required along with low power consumption. It can be offered by single-chip approach [2].

In this paper, we describe the circuit design and performance of a 1-5GHz low-power single-chip receiver IC for an optical video distribution system.

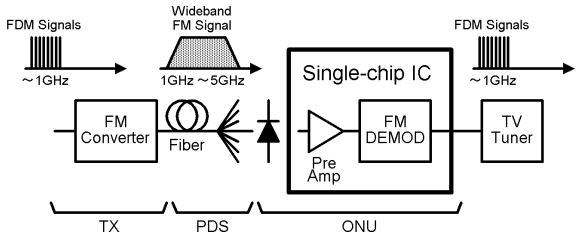


Fig. 1. Multichannel video transmission system using super wideband FM scheme.

II. BLOCK DIAGRAM

Fig.2 shows the block diagram of the developed IC. The IC consists of a transimpedance amplifier (Pre AMP), a limiting amplifier and a complete delay-line type FM demodulator, except for the required PIN photo-diode (PD).

An optical signal is converted to an electrical current signal by the PIN photo-diode. Next, the preamplifier converts the input current signal to a voltage signal. Finally, the limiting amplifier limits the output voltage swing to prevent waveform distortion.

A delay-line type FM demodulator is employed to convert a wideband FM signal back to original FDM signals. By adding the pulse signal with its delayed signal (from the delay-line circuit), a constant pulse width and the pulse density in proportion to the input frequency are obtained. The pulse width of the output signal is τ, since the delay time is τ as shown in Fig.2. Finally, the original FDM signals are obtained after routing the signal through a low-pass filter (LPF).

It is important for the IC to prevent waveform distortion. In addition, the pulse period and width are 200ps and less than 100ps, respectively, with input frequencies up to 5GHz. Therefore, a broadband, flat gain response, combined with small group-delay deviation and very fast operation without waveform distortion, are required for the IC in addition to low power consumption.

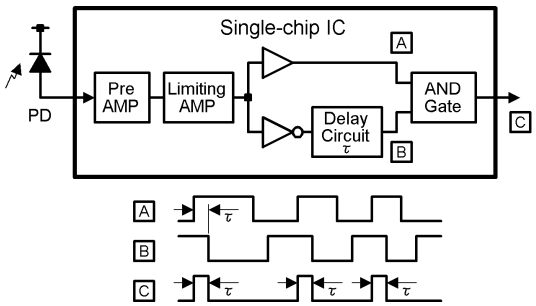


Fig. 2. Block diagram of the developed IC.

III. CIRCUIT DESIGN

Broadband and flat frequency response of the gain and group delay are important parameters for the circuit design. In addition, transient response such as ringing must also be prevented. Then, the IC is designed to achieve these characteristics with minimum power consumption.

A. Preamplifier

Fig.3 shows the circuit schematic of the preamplifier. The preamplifier is a two-stage architecture, which consists of a common-emitter amplifier (Q1, R1, R2) for the input stage and an emitter-follower (Q3) for the output stage.

The feedback resistor Rf is used for current-to-voltage conversion. The use of a negative feedback technique allows the amplifier's bandwidth to be extend as well as setting the transimpedance gain accurately. The transimpedance gain is mainly determined by the value of the feedback resistor Rf, rather than performance characteristics of the transistor.

Since the high drive capability is required for the output stage, a large transistor is needed. However, the frequency response is reduced, because of the increased input capacitance, which result from the larger transistor. Then, another emitter-follower (Q2) is inserted into the feedback loop. As a result, the frequency response is improved by the small input capacitance of Q2, maintaining the high drive capability. In addition, the influence on input capacitance of Q3 is also decreased, since the input signal is divided by R1 and R2.

This single-chip solution also has the additional advantage of eliminating the parasitic capacitance of the wiring which typically connects the preamplifier to the demodulator.

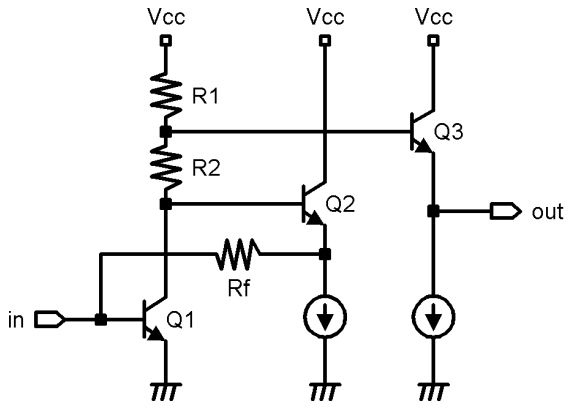


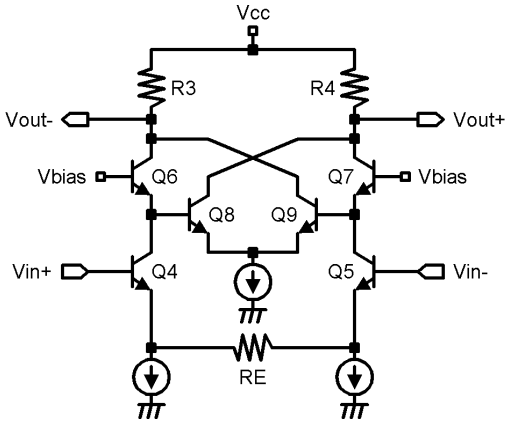
Fig. 3. Circuit schematic of the preamplifier.

B. Limiting Amplifier and Delay Circuit

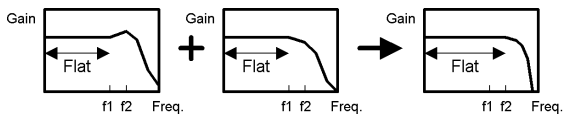
A current gain cell, as shown in Fig.4(a), is used for the limiting amplifier and the delay circuit. There are no bandwidth limitations due to charging and discharging of the input capacitance because of its current amplification. Therefore, this current gain cell is suitable for use as a broadband amplifier.

Next, the flat frequency response of the gain and group delay is improved by combining amplifiers which have different frequency responses as shown Fig.4(b). Since the frequency response of the amplifiers is determined by bias current, transistor size, load impedance, etc., careful analysis of the frequency response is used to determine the optimum parameter and combination of the amplifiers.

Also, an emitter resistor RE is used to increase the input impedance of the current gain cell to prevent ringing. The ringing of the emitter-follower's output signal is created by two components: the inductive portion of the emitter-follower's output impedance, and the capacitive portion of the differential amplifier's input impedance. Ringing is very undesirable. Because, the delay circuit's delay time is vary according to input frequency, so that the pulse width of the AND gate's output waveform does not become constant. These effects cause distortion and noise of the FM demodulator. However, since adding an emitter resistor decreases the gain of the amplifier, the value of emitter resistor RE is optimized to obtain the best trade-off between decreased ringing and decreased gain.



(a) Circuit schematic of the current gain cell.



(b) Frequency response of combined amplifiers.

Fig. 4. Limiting amplifier and delay circuit.

C. AND Gate

Fig.5 shows the circuit schematic of the AND gate. An OR gate circuit is used to create the AND gate circuit, in order to improve the distortion and frequency response. In addition, the use of an OR gate circuit has the advantage of low voltage operation, since a number of cascode transistors can be removed from the circuit schematic.

Because parasitic capacitance, such as collector-base capacitance Cbc, can create cross-talk between input signals, the waveform at the collector of transistor Q11 has some noise spikes (see signal "a" in Fig.5). On the other hand, the waveform at the collector of transistor Q12 does not have noise spike, since the voltage at the base of transistor Q12 is held constant. Therefore, the output signal of the AND gate is taken from the collector of transistor Q12 to prevent the degradation in the output signal waveform.

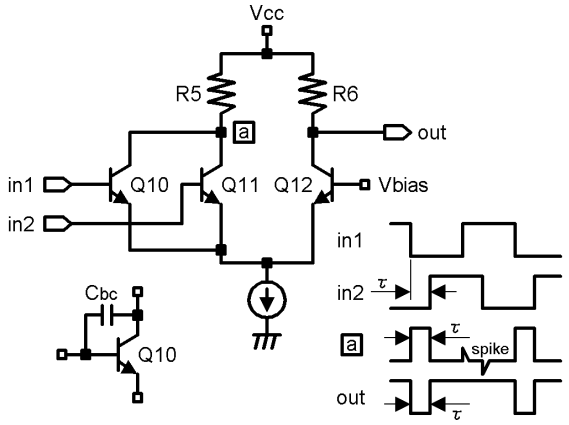


Fig. 5. Circuit schematic of the AND gate.

IV. PERFORMANCE

Fig.6 shows the microphotograph of the IC. The IC is fabricated using 0.5μm silicon bipolar technology. Die size is 2.4 x 2.4mm.

The characteristics were measured with die form mounted on an alumina substrate using flip-chip bounding techniques. The frequency response of the preamplifier is shown in Fig.7(a). The transimpedance gain at 1GHz is 44dBΩ, and the equivalent input noise current density is 16pA/√Hz as average from 1 to 5GHz. Fig.7(b) shows the input frequency vs. output voltage characteristics (f-v characteristics) of the IC. The linear characteristic is obtained up to 5GHz, with a FM demodulation efficiency of 7mV/GHz.

Power consumption is 0.73W at a power supply voltage of 3.0V. This is one of the smallest power consumption figures ever reported for such an IC. The electrical characteristics are summarized in Table I.

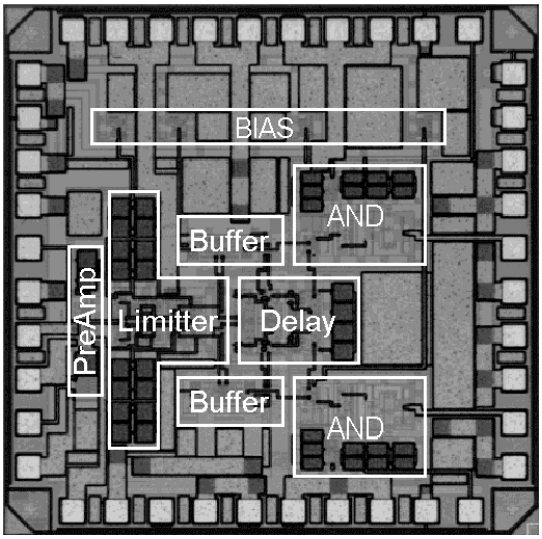
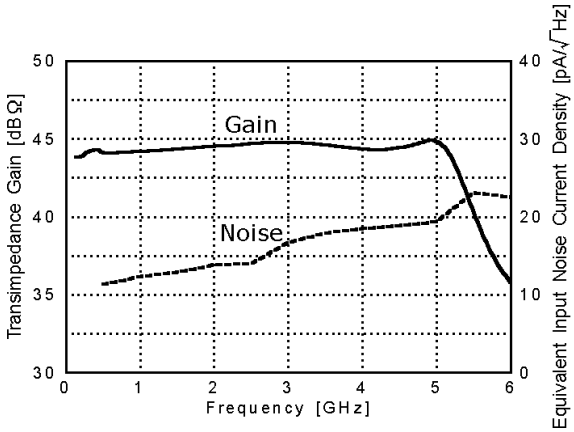
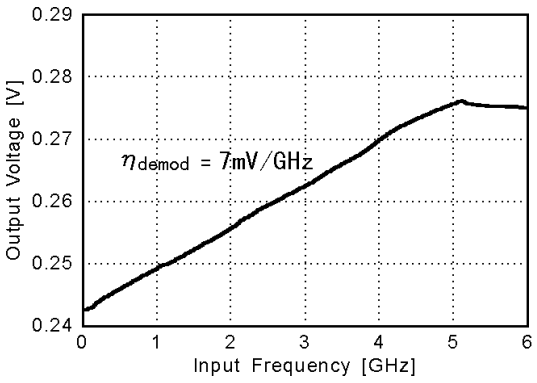


Fig. 6. Microphotograph of the fabricated IC.



(a) Frequency response of the preamplifier.

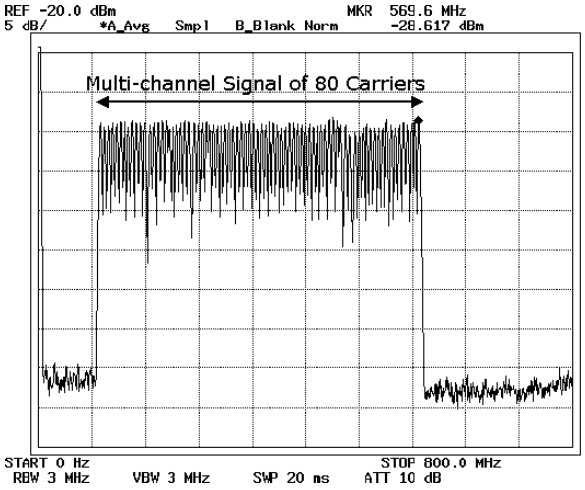


(b) f-v characteristics of the IC.

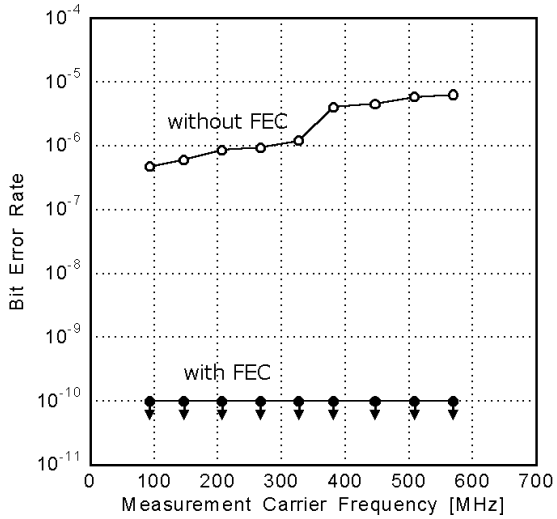
Fig.7 Measurement results.

TABLE I Electrical Characteristics.

Frequency Response	1-5 GHz
FM Demodulation Efficiency	7mV/GHz
Power Consumption	0.73W
Supply Voltage	3.0V
Die Size	2.4 x 2.4mm



(a) Demodulated spectrum.



(b) Bit error rate.

Fig. 8. Measurement results using a wideband FM.

The demodulation characteristics were measured by applying a wideband FM signal, which was modulated by a multi-channel signal of 80 carriers. The demodulated spectrum is shown in Fig.8(a). The bit error rate (BER) is shown in Fig.8(b). The BER was measured using 64-QAM modulated signals for each of the 80 carriers. The BER is less than $1x10^{-5}$ without forward error correction (FEC) and error-free (less than $1x10^{-10}$) with FEC.

V. Conclusion

A broadband single-chip FM receiver IC for an optical video distribution system has been successfully developed. Broadband frequency response and low power consumption have been realized by sophisticated circuit design in consideration of the trade-offs between low voltage operation and high performances. Transmission for 320-channels of MPEG-2-encoded digital video signal (4-channel/carrier) is achieved lower BER than $1x10^{-10}$ by using the developed IC. The IC is suitable for an optical video distribution system, which has different modulation schemes as well as simultaneous transmission such as VSB-AM and 64-QAM.

Acknowledgement

The authors would like to thank T. Nakamura, M. Hanabusa, Y. Miyahara, and H. Asano for his continuous encouragement through this work. The authors are also grateful to the colleagues at Matsushita Communication Industrial Co., Ltd.

References

[1] K.Kikushima et al., "150-km Non-Repeated 60-channel AM-Video Transmission Employing Optical Heterodyne AM/FM Converter", ECOC'95, Th.L.3.1, 1995

[2] Satoshi Ikeda et al., "Small ONU module for FM converted multichannel video signal transmission systems", OFC'98, ThT4